What is claimed is:

1. A switch, comprising:

a first stage having a plurality of first switch circuits, each of said plurality of first switch circuits having a plurality of inputs and a plurality of outputs;

a second stage having a plurality of second switch circuits, each of said plurality of second switch circuits having a plurality of inputs, each of which being respectively coupled to one of said plurality of outputs of each of said plurality of first switch circuits, and a plurality of outputs, a number of said plurality of second switch circuits equaling N, where N is an integer other than a power of 2; and

a third stage having a plurality of third switch circuits, each of said plurality of third switch circuits having a plurality of inputs and a plurality of outputs, each of said plurality of inputs of each of said plurality of third switch circuits being coupled to a respective one of said plurality of outputs of each of said plurality of second switch circuits.

2. A switch in accordance with claim 1, wherein said switch is a non-blocking switch.

3. A switch in accordance with claim 1, wherein said first, second and third pluralities of switch circuits are configured in accordance with a Looping Algorithm.

4. A switch in accordance with claim 1, wherein each of said pluralities of first and third switch circuits are configured to be logically represented as respective groupings of 2 x 2 switches.

5. A switch in accordance with claim 1, wherein each of said plurality of outputs of said plurality of first switch circuits, outputs of respective one of a plurality of data signals, said data signals being time-division multiplexed.

6. A switch in accordance with claim 5, wherein said each of said plurality of data signals includes a plurality of groups of time slots, each of said plurality of groups further including a plurality of subgroups of time slots.

7. A switch in accordance with claim 6, wherein each of said plurality of second switch circuits is configured as a plurality of logical sub-switch circuits, each of said plurality of sub-switch circuits being configured to direct selected subgroups of time slots among different groups to one of said plurality of outputs of said plurality of second switch circuits.

8. A switch in accordance with claim 7, wherein a number of said plurality of logical sub-switch circuits in each of said plurality second switch circuits equals a number of said plurality of subgroups within each group of time slots.

9. A switch in accordance with claim 7, wherein each of said plurality of logical sub-switch circuits includes a demultiplexer coupled to selected ones of said plurality of inputs of said plurality of second switch circuits and a multiplexer coupled to selected ones of said plurality of outputs of said second switch circuits, said demultiplexer being configured to separate said plurality of subgroups from different first groups, and said multiplexer being configured to combine said selected ones of said subgroups in a predetermined manner to supply second groups of time slots.

10. A switch in accordance with claim 1, further comprising:

a plurality of optical receiver circuits coupled to said plurality of inputs of said first switches; and

a plurality of optical transmitter circuits coupled to said plurality of outputs of said third switches.

11. A switch in accordance with claim 1, wherein said plurality of second switches are configured to be represented as n logical switches, where n is a power of 2.

12. A data transmission method, comprising the steps of:

routing said data through a first switch stage, said first switch stage including a plurality of first switch circuits, said first switch circuits being configured to be logically represented as a first plurality of 2 x 2 switches;

routing said data through a second switch stage, said second switch stage having N switch circuits, where N is other than a power of 2; and

routing said data through a third switch stage, said third switch stage including a plurality of third switch circuits, said third switch circuits being configured to be logically represented as a second plurality of 2 x 2 switches.

13. A method in accordance with claim 12, further comprising the step of:

reconfiguring said first, second and third switch circuits in accordance with a looping algorithm.

14. A method in accordance with claim 12, wherein said step of routing said data through said second switch stage further comprises the step of time-division multiplexing said data.

15. A method in accordance with claim 14, further comprising the steps of:

grouping said data into a plurality of frames, each of said frames including a plurality of subgroups, each of said subgroups including a plurality of time slots;

said step of routing said data through said second stage of switches, comprising the steps of:

demultiplexing a first frame into constituent first subgroups;

demultiplexing a second frame into constituent second subgroups;

multiplexing at least one of said first subgroups and at least one of said second subgroups into a third frame.